REMARKS

This is in response to the Office Action dated February 7, 2007. Examiner rejected all the claims 1-35, under 35 USC 103(a). Examiner also raised some claims objections. The claims objections will be discussed first.

Regarding claim 1, Examiner objected to the claim as being in confused form such as what elements of the claim belong to "comprising" and what elements belong to "including". In order to overcome this objection, Applicants have canceled claim 1 and have written it as newly submitted claim 36, with a view to overcoming this objection.

Regarding claim 1, Examiner objected to inclusion of FIFO register, as not supported by the specification. Reconsideration of this objection is requested. Those skilled in the art understand a FIFO (first in first out) to be a FIFO register, shift register, or the like. For example, these terms are used interchangeably throughout the companion patent application serial number 10/029,709, filed on the same date as this application. Note further that in the instant application at paragraph [0026], FIFO is also referred to as FIFO buffer 522, a "buffer" also being used interchangeably with "register". If Examiner would consider it helpful, Applicants would be willing to make an amendment to the drawing and/or specification to add "register" after "FIFO" in an appropriate place to achieve literal consistency. However, this should not be necessary because as illustrated in FIG. 5 and recited in originally filed claim 1: "a FIFO register (522) receiving a parallel data input and outputting a signal to said phase detector 518" must necessarily refer to FIFO 522. It is respectfully submitted that FIFO 522 illustrated in FIG. 5 and described in the specification fully supports "FIFO register" recited in claim 1. For these reasons, the term "FIFO register" has been retained in claim 36; which has been written to replace canceled claim 1.

Claim 17 has been objected to because "Examiner does not clearly understand what part of the claim is preamble and limitations". Apparently, there is objection to "comprising:" being recited twice. Claim 17 has been amended to overcome this objection.

Claims 1-3 and 6-9 have been rejected under 35USC 103 as being unpatentable over 5 references as follows: Gu (US 6,901,126) in view of Filip (US 6,081,572) in view of Drost et al (US 6,194, 929) in view of Song (US 6,639,956) and further in view of Schatz et al (US 6,744,787). Claims 4-5 have been rejected under 35USC103 as being unpatentable in view of the aforementioned 5 references plus Kirlpatrick (US 6,476,681). Claims 17-18 have been rejected under 35USC103 as being unpatentable in view of the aforementioned 5 references plus Miller et al (US 6,316,976) and Schmid et al (US 6,735,291).

Claims 19-22 have been rejected under 35USC 103 as being unpatentable in view of all 8 aforementioned patent references. Claims 10-11, 16, 23-35 have been rejected under 35 USC 103 as being unpatentable over the following 8 references, to wit, Gu-Filip-Drost-Song-Schatz in view of Lennen (US 5,805,108), Jaffe et al (US 2001/0034867) and Scala et al (US 4,551,689). Claims 12-13 have been rejected under 35USC 103 as being unpatentable over the aforementioned 8 references, to wit, Gu-Filip-Drost-Song-Schatz-Lennen-Jaffe-Scala in view of a ninth reference: Kirkpatrick (US 6,476,681).

Claims 14-15 have been rejected under 35USC103 as being unpatentable over the aforementioned 8 references, to wit, Gu-Filip-Drost-Song-Schatz-Lennen-Jaffe-Scala in view of a ninth reference: Clark (US 6,323,910). In addition, certain claims received multiple rejections over the same references with similar rationale. All the rejections are believed to be overcome by the amendments and explanations submitted herein.

Applicants note at the outset that there is no way that anyone skilled in the art would have assembled the aforementioned grouping of references (up to 9 documents) without having knowledge of Applicants' teachings. There can be no other reason for bringing all these references together. Although the Supreme Court has recently raised a question about the "motivation test" for assembling references to raise a question of obviousness, the long list of assembled patents cannot withstand any test. In fact, as will be noted hereinbelow, none of the references address the problem solved by Applicants with the solution claimed as Applicants' invention.

Gu (US 6,901,126) has been cited by Examiner as the primary reference. Indeed, by its disclosure of a dual loop system (PLL and DLL), albeit in a receiver and not a transmitter application, it appears to be the only reference relevant to Applicants' invention. For this reason, Applicants will now describe the reasons that the Gu teachings fail at the point of novelty. When the primary reference fails to disclose Applicants invention and that invention is not disclosed in any other reference, then the claimed invention cannot be said to be obvious.

Prior to a discussion of the amended claims, significant generic conceptual distinctions between the instant application and Gu US 6,901,126 should be noted. It is agreed with Examiner that Gu discloses the use of a dual loop clock recovery system. In the nomenclature of Gu, this structure is used in the receiver of a TDM system. Structurally, this specifies that the input to the phase detector in the DLL be connected to a signal containing the relationship between the received input data and the receive clock. See FIG. 3 of Gu illustrating PHASE SELECT CIRCUIT/FILTER 42 (the phase detector) receiving an input from DATA RECOVERY 40, where the early/late signals are the relationship between the received data and receive clock.

Although the Gu disclosure mentions a transceiver (both transmitter and receiver) at col. 3, line 35, the Gu teaching is directed only to a receiver. Gu specifically notes at column 3, lines 35-37 that his transceiver uses a: conventional PLL 30 frequency synthesizer on the Transmit side. However, this statement appears in reference to FIG. 3; which is described as a block diagram of a time division multiplex data recovery system (Col 2, lines 46-47) i.e. a receiver. Thus, it is clear that Gu's invention relates to solving a problem in the receiver. For this reason the DLL bandwidth is set to track the jitter on the received input. Accordingly, in the Gu apparatus, narrow bandwidth is not desirable, because it reduces the jitter tolerance of the clock recovery circuit. The clock must be allowed to track the input jitter in order to be able to clock the data in the middle of the data eye (i.e the clock timing must change as fast as the data timing changes.) Gu does not tout the wide bandwidth tracking capability, just the power savings of having a narrower band width loop.

In contradistinction to the teachings in Gu, Applicants' dual loop data serializer is (in the nomenclature of Gu) a transmitter and claim 1 is directed to a transmitter. Applicants' novelty is in the transmitter: "wherein the phase detector in the DLL compares the received clock with the transmit clock" (aka synthesized clock in the specification). The utilization, interaction and purpose of the dual loops in Applicants' invention are different from that in Gu and the other prior art. In contradistinction to the prior art, the present invention teaches that the DLL bandwidth sets the jitter bandwidth on the transmit output. In this case, narrow bandwidth is desirable because the desired result is to retime a high jitter input and produce a low jitter output. (This has been described as jitter filtering.) In order to accomplish this desired result, a FIFO is used to store the received data and to provide retransmission with a clean clock. FIFO's (aka FIFO registers, FIFO buffers, etc.) were well known in the prior art prior to Applicants' invention. However, they were not known in a data serializer (transmitter) in a combination where the phase detector in the DLL compares the received clock with the transmit clock.

The primary reference (Gu) does not include a FIFO register; which is an important feature of Applicants' invention. To overcome this deficiency in the Gu reference, Examiner cites Song as a teaching of a connection between a phase detector and a FIFO register (noting column 6, lines 7-60). However, other than the recitation of a FIFO, neither the cited portion nor any other portion of Song reveals any relationship to Applicants' invention. Simply stated, neither Gu nor Song suggest combining the teachings of Gu with the teachings of Song to create the combination of a FIFO and dual loop elements co-acting functionally to achieve the result as recited in newly added claim 36. Moreover, as noted herein, even if Gu and Song were combined legitimately, the combination would not result in Applicants' invention because neither reference addressed or solved the same problem as Applicants.

As is well accepted patent law, most circuit patents are combinations of known circuit elements and/or combinations of known groups of circuit elements (such as flip-flops, logic circuits, etc.) One test for patentability then becomes: Does the newly invented combination differ from the prior art by virtue of its structure, operation, and

result? In particular, it is necessary to note whether or not the newly invented combination addresses and solves a problem in a novel and unobvious way. It is respectfully noted, that the present invention having a phase detector that compares the received clock with the transmit clock utilizes a dual loop for a different purpose, with a different structure and mode of operation in a different portion of a plesiochronous system than suggested by any of the prior art. As set forth in newly submitted claim 36, the present invention is novel and unobvious.

36. (New) In a plesiochronous system, a dual loop data serializer comprising:

a first-in-first-out (FIFO) register receiving a parallel data input and a data clock input and providing a plurality of outputs;

a parallel-in serial-out (PISO) serializer coupled to one of the plurality of outputs of said FIFO register, receiving an input signal from said FIFO register, and outputting serialized data;

a phase detector, having an input coupled to an output of said FIFO register, for receiving a signal representative of the fill rate of said FIFO register, said phase detector providing an output;

a narrow band loop filter having an input coupled to the output of said phase detector and configured to provide an output to a phase shifter, thereby producing a phase shift in a PLL;

a phase shifter having a first input coupled to the output of said narrow band loop filter and providing an output;

a phase/frequency detector having an input for receiving the output of said phase shifter and also receiving a local reference input, and providing an output;

a wideband loop filter having an input coupled to the output of the phase/frequency detector to suppress phase noise and providing an output;

a voltage controlled oscillator (VCO) having an input coupled to the output of said wideband loop filter, and providing a synthesized clock to said PISO serializer and also to a second input of said phase shifter;

said phase shifter, phase/frequency detector, and wideband loop filter forming a phase locked loop with the VCO, such that the phase and frequency of the output of the VCO is modified by the output of the narrow band loop filter; and

said PISO serializer providing the synthesized clock to said FIFO register;

whereby said phase detector compares the received clock with the synthesized clock.

Starting with the preamble, Applicants recite use in a plesiochronous system, a dual loop data serializer. As previously noted, this serializer is a transmitter and not the receiver described in Gu, for example at FIG. 3. Then, Applicants recite a FIFO, which admittedly is missing in Gu. As noted hereinabove, the mere noting of a FIFO as part of a bill of materials from another reference (Song) cannot raise a question of obviousness of Applicants' invention. The same argument should overcome the validity of using another reference showing a PISO to overcome the failing of Gu to include such structure in his teaching.

The next element recited in the claim is:

a phase detector, having an input coupled to an output of said FIFO register, for receiving a signal representative of the fill rate of said FIFO register, said phase detector providing an output;

Although Gu discloses a phase detector, in Gu it is not connected the same way and is not used for the same function as in Applicants' invention. The same arguments urged for patentability with respect to the just described elements are similarly applied to each of the other elements in claim 36, to wit:

a narrow band loop filter having an input coupled to the output of said phase detector and configured to provide an output to a phase shifter, thereby producing a phase shift in a PLL;

a phase shifter having a first input coupled to the output of said narrow band loop filter and providing an output;

a phase/frequency detector having an input for receiving the output of said phase shifter

and also receiving a local reference input, and providing an output;

a wideband loop filter having an input coupled to the output of the phase/frequency detector to suppress phase noise and providing an output;

a voltage controlled oscillator (VCO) having an input coupled to the output of said wideband loop filter, and providing a synthesized clock to said PISO serializer and also to a second input of said phase shifter;

said phase shifter, phase/frequency detector, and wideband loop filter forming a phase locked loop with the VCO, such that the phase and frequency of the output of the VCO is modified by the output of the narrow band loop filter; and

said PISO serializer providing the synthesized clock to said FIFO register;

Referring to FIG. 5, note that the synthesized clock (clean transmit clock) outputted by VCO 514 is coupled (through PISO serializer 524) into FIFO 522. The dynamic difference in the phase/frequency of the data clock and synthesized clock is provided to phase detector 518 providing a comparison of the received clock and transmit clocks as now recited in claim 36, as follows:

whereby said phase detector compares the received clock with the synthesized clock. (emphasis added)

With the overall combination, Applicants achieve a result by which a comparison of the received clock with the transmit (synthesized) clock provides the desired transmission characteristics. Neither the combination of elements nor the particular co-action of elements resulting in the solution of a problem addressed by Applicants Is found in the cited prior art. Again, it is respectfully pointed out that the mere existence of the elements (in a large number of prior art references solving different problems with different solutions) is not sufficient to raise a question of obviousness under 35USC103..

Accordingly, claim 36 is believed to be allowable and claims 3-7 and 9 depending from claim 36 are believed to be allowable for the same reasons. Claims 1, 2, and 8 have been canceled. In addition, claims 3-7 and 9 recite additional features, as follows:

3. (Currently amended) The data serializer of claim 36 ~~1~~, wherein said PLL locks to said signal from said FIFO to said phase detector.

4. (Currently amended) The data serializer of claim 36 ~~1~~, wherein said wideband loop filter ~~of said PLL~~ comprises a wideband analog filter to suppress VCO phase noise and generate a low jitter clock.

5. (Currently amended) The data serializer of claim 36 ~~1~~, wherein said narrow band loop filter ~~of said DLL~~ comprises a digital narrow band filter to filter noise from the data clock and set the jitter bandwidth..

6. (Currently amended) The data serializer of claim 36 ~~1~~, wherein said signal representative of the fill rate of said FIFO register and inputted to said phase detector comprises a FIFO fill level indicator.

7. (Original) The data serializer of claim 6, wherein said phase detector is configured to translate said FIFO fill level into a digital value.

9. (Currently amended) A dual loop retimer comprising the data serializer of claim 36 ~~1~~.

These additional features of claims 3-7 and 9 are self explanatory and should require no further detailed explanation.

Regarding claim 10, after a rejection over 6 references, Examiner correctly noted that a still further reference, to wit, Jaffe was needed to show applying a filtering method to a FIFO and a still additional reference, Scala allegedly disclosing a method of using a phase shifter to lower phase noise signal (abstract) would be required to complete a bill of materials to raise a question of obviousness. In addition to the prior discussion pointing out that a bill of materials from 8 different patents is inappropriate to raise a question of obviousness, it is noted again that none of the references suggest the co action of Applicants' invention leading to Applicants' result. The references fail

individually, as well. For example, in contradistinction to Scala, Applicants reduce phase noise with their wide bandwidth filter and NOT the alleged Scala method of using a phase shifter to lower phase noise signals. Lastly, none of the references related to data serialization (transmission) in a plesiochronous system, as recited in amended claim 10, reproduced here, as follows:

10. (Currently amended) In a plesiochronous system, a ~~A~~ method for PLL/DLL data serialization comprising:

detecting a local reference at a phase/frequency detector (PFD) of a phase lock loop (PLL);

phase locking a voltage controlled oscillator (VCO) of said PLL to a local reference to suppress a phase noise of said VCO;

receiving a parallel data input and a data clock at a FIFO register;

filtering, at a delayed lock loop (DLL), a signal representative of a fill level of said FIFO;

phase shifting an output of said VCO of said PLL in response to said filtering step;

locking said PLL to a frequency corresponding to a pre-filtered signal input to said DLL;

receiving, at a parallel-in serial-out (PISO) serializer, said parallel data and said VCO output; and

outputting a serialized data from said PISO serializer with said VCO output a transmit clock.

Since the claimed method steps are not suggested by the cited prior art, claim 10 is believed to be allowable. Claims 11-15, depending on claim 10 are believed to be allowable for the same reasons and also as they recite additional features of the invention. For example, claim 11 recites the step of outputting a synthesized clock.

Regarding claim 17, after a rejection over 5 references, Examiner correctly noted that a still further reference, to wit, Miller was needed. But all Miller teaches is that

DDLL's existed before Applicants' invention. Then, Examiner added the Schmid reference as including a SIPO shift register and PISO shift register. Examiner notes that in Schmid, these components are used to transmit from non-secure to secure channels, specifically referencing column 9, lines 30-35 where the FPGA 518 components are described. In addition to previous comments herein addressing the inappropriateness of combining a large number of references to develop a bill of materials, Applicants respectfully submit that they neither addressed the problem nor the solution of the problem of transmitting from non-secure to secure systems. The mere pre-existence of SIPO and PISO shift registers is insufficient to render Applicants' claim 17 unpatentable. The inventory of parts represented by the cited references nowhere teaches the method disclosed for the first time by Applicants and claimed as their invention.

Claims 18-22 depend from claim 17 and are believed to be allowable for the same reasons and also that additional features are recited. Examiner has cited additional references (Kirkpatrick US 6,476,681). However, Kirkpatrick merely teaches an adjustable bandwidth phase locked loop. At column 2, lines 32-44, Kirkpatrick teaches that a variable loop filter may include a narrowband loop filter, a wideband loop filter and a switch which switches the narrow band filter between the phase-locked loop and the voltage controlled oscillator in accordance with receipt of a bandwidth adjustment signal. However, in Applicants' invention, although a narrow band loop filter and a wideband loop filter are used, there is no switching involved and the positioning and purpose of Applicants' filters is not suggested by Kirkpatrick. Accordiongly, it is respectfully submitted that the addition of Kirkpatrick to the list of references is inoperative to raise a question of obviousness. Therefore, claims 17-22 should be allowed.

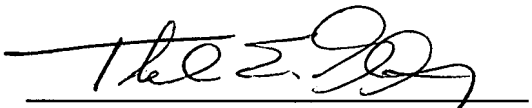
Claims 23 and 29 were rejected on the same rationale as claims 1 and 17 and the foregoing explanation regarding the reasons for allowing claims 36 and 17 are believed to justify the allowance of claims 23 and 29, as well.

Claims 24-28 depend from claim 23 while claims 30-35 depend from claim 29. These claims are believed to be allowable for the same reasons and also because they

recite additional features of the invention. With the foregoing explanation regarding the allowability of the independent claims, these dependent claims are also believed to be allowable.

In conclusion, claims 1, 2, 8, and 16 have been canceled and claim 36 has been newly submitted. Claims 3-7, 9-15, and 17-36 (all the claims) are believed to be allowable in view of the herein discussed amendment and rationale. Examiner is respectfully requested to telephone the undersigned if there is a question or if such would further the prosecution of this application. An early notification of allowance is earnestly solicited.

Respectfully submitted,
Benjamim TANG et al



Attorney for Applicants
Theodore E. Galanthay
Attorney Reg. No, 24,122

From: Primarion, Inc.
PO Box 28308
Scottsdale, AZ 85255-0155

Telephone: 480-575-0744

TEG/cw